34. A semiconductor device according to Claim 33, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

35. A semiconductor device according to Claim 34, wherein the metal silicide layer has a thickness of 5-20 nm.

36. A semiconductor device according to Claim 33, wherein said substrate includes a semiconductor substrate.

B' cont.

37. A semiconductor device according to Claim 33, wherein the gate electrode is provided above a principal surface region of a semiconductor substrate, covering the spacing between a source region and drain region of the MOS transistor, the source and drain regions each having a first diffusion layer and a second diffusion layer, the second diffusion layer having a junction depth extended into the substrate deeper than that of the first layer.

38. A semiconductor device according to Claim 37, wherein the silicon layer is a polycrystalline silicon layer doped with an impurity of n-type or p-type conductivity.

39. A semiconductor device according to Claim 38, wherein the metal silicide layer has a thickness of 5-20 nm.

B' Cont

40. A semiconductor device according to Claim 37, wherein said substrate includes a semiconductor substrate.